

CMOS-8L 3 Volt, 0.5-Micron CMOS Gate Array

Description:

NEC's CMOS-8L is an optimized true 3-Volt technology, targeted for applications requiring extensive integration, low power and high speed. The CMOS-8L ASICs are ideal for use in applications like notebooks or handheld devices, engineering workstations (EWS), graphics, telecom and LAN products.

The 28 CMOS-8L masters are available in a wide variety of package types and two or three metallization layers in a sea-of-gates architecture.

New library blocks such as PLL (Phase-Locked-Loop), GTL (Gunning Transceiver Logic) and PCI interfaces are available. 5 V signal interfacing is possible with special macros. The CMOS-8L libraries are fully compatible with CMOS-6 and CMOS-8 libraries.

Features:

- True 3 V, 0.5 μm (drawn) CMOS process
- Very high speed at 3 V operation
- Low power consumption
- Ultra-high pin count
- 5V Signal interface
- Variable output drive (1 to 24 mA)
- New library blocks like PLL and GTL
- Compiled RAM / ROM
- Wide range of package options
- Supports scan test methodology

Product Outline

Master ($\mu\text{PD65..}$) 2 Layer	840	841	842	843	845	846	848	849	850	851	852	853	855	858
Master ($\mu\text{PD65..}$) 3 Layer	860	861	862	863	865	866	868	869	870	871	872	873	875	878
Gate Count (raw)	10921	20832	30192	40592	52528	61904	81984	102272	120768	148256	202752	255744	342000	488720
Number of pads ^{Note1}	148	188	196	228	260	284	324	364	396	436	508	572	660	788
Utilisation (Minimum)	65% for 2 metal layers, 80% for 3 metal layers													
Toggle frequency (Min.)	175 MHz													
Delay time	Internal gate	0.13 ns (F/O = 1, l = 0 mm); 0.21 ns (F/O = 2, l = 2 mm) ^{Note2}												
	Input buffer	0.40 ns (F/O = 2, l = 2 mm)												
	Output buffer	1.67 ns ($C_L = 15 \text{ pF}$)												
Consumed Power	Internal gate	1.33 $\mu\text{W}/\text{MHz}/\text{Cell}$ (3.3 V), 0.8 $\mu\text{W}/\text{MHz}/\text{Cell}$ (3.0 V)												
	Input buffer	3.87 $\mu\text{W}/\text{MHz}/\text{Cell}$ (normal buffer)												
	Output buffer	0.2 mW/MHz/Cell ($C_L = 15 \text{ pF}$)												
Power supply voltage	3 V $\pm 10\%$, 3.3 V $\pm 0.3 \text{ V}$													
Operating temperature	-40 to +85°C													
Interface level	3 V / 5 V CMOS level, TTL level, GTL, PCI													
Technology	Channelless (Sea-of-Gates) 0.5 μm Silicon gate CMOS, 2 or 3 Al-Metal layers													

Note 1: Including power supply and GND. Number of pins which can be used for signals depends on package

Note 2: 2-input NAND power gate

Design Tool Support

The low power gate array family CMOS-8L is fully supported by NEC's advanced ASIC design environment OpenCAD[®] - a unified design package for front-to-back-end. This system allows designers to combine tools from the CAE industry's most popular third-party vendors and from NEC's offer of powerful proprietary software tools.

The OpenCAD[®] integration system supports tools for schematic capture, logic synthesis, floorplanning, automatic test pattern generation (ATPG), full timing simulation, accelerated fault-grading and advanced place-and-route algorithms.

The company's proprietary clock tree synthesis tool can be used to automatically buffer the clock lines to minimize clock skew. The non-linear delay calculator ensures timing accuracy throughout the simulation, synthesis, and silicon stages. These advanced CAD tools help ensure accurate designs.

CrossCheck[®] Test Option

Additional to CMOS-8L NEC offers the CMOS-8LCX family with CrossCheck[®] test option. This technology gives full observability and controllability for a minimum of additional silicon area. For further information please refer to the CMOS-8LCX Data Sheet.

Electrical Characteristics

Absolute Maximum Ratings

Parameters	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		-0.5 to +4.6	V
Input/Output voltage	V_I/V_O	3 V interface	-0.5 to +4.6 $V_{I/O} < V_{DD} + 0.5$	V
		5 V interface	-0.5 to +6.6 $V_{I/O} < V_{DD} + 3.0$ V	V
Output current	I_O	$I_{OL(MIN)} = 3.0$ mA	10	mA
		$I_{OL(MIN)} = 6.0$ mA	20	mA
		$I_{OL(MIN)} = 9.0$ mA	30	mA
		$I_{OL(MIN)} = 12.0$ mA	40	mA
		$I_{OL(MIN)} = 18.0$ mA	60	mA
		$I_{OL(MIN)} = 24.0$ mA	80	mA
Operating temperature	T_{opt}		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Input/Output Capacitance ($T_a = +25$ °C, $V_{DD} = 0$ V)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$f = 1$ MHz		10	20	pF
Output capacitance	C_{OUT}	Unmeasured pins clamped to 0 V		10	20	pF
I/O capacitance	$C_{I/O}$			10	20	pF

Recommended Operating Conditions (3.3 V \pm 0.3 V, 3.0 V \pm 10%)

Parameters	Symbol	MIN.	MAX.	Unit
Power supply voltage	V_{DD}	2.7	3.6	V
Input voltage	V_I	0	V_{DD}	V
Ambient temperature	T_a	-40	+85	$^{\circ}$ C
High-level input voltage (3 V)	V_{IH}	2.0	V_{DD}	V
Low-level input voltage (3 V)	V_{IL}	0	0.8	V
High-level input voltage (5 V)	V_{IH}	2.0	5.5 V	V
Low-level input voltage (5 V)	V_{IL}	0	0.8	V
Positive Trigger voltage	V_P	1.7	2.7	V
Negative trigger voltage	V_N	0.6	1.2	V
Hysteresis voltage	V_H			V
Input rise or fall time	t_r, t_s	0	200	ns
Input rise or fall time, Schmitt	t_r, t_s	0	10	ms

Note: The rise/fall times given for a Schmitt trigger input buffer vary depending on the operating environment. Simultaneous switching of output buffers should be analyzed carefully.

AC Characteristics ($T_a = -40$ to $+85^{\circ}$ C)

Parameters	Symbol	Conditions	3.0 V \pm 10%			3.3 V \pm 0.3 V			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Toggle frequency	f_{tog}	Internal toggle F/F (F/O = 2)	175			175			MHz
Propagation delay	t_{PD}	Internal gate F/O = 1, l = 0 mm F/O = 2, l = 2 mm		0.20 0.40			0.18 0.33		ns ns
		Internal gate (Power gate) F/O = 2, l = 2 mm		0.29			0.21		ns
		Input buffer F/O = 2, l = 2 mm					0.40		ns
		Output buffer (FO01), $C_L = 15$ pF		1.92			1.70		ns
Output rise time	t_r	Output buffer (FO01), $C_L = 15$ pF		1.95			1.76		ns
Output fall time	t_f	Output buffer (FO01), $C_L = 15$ pF		1.55			1.39		ns

DC Characteristics ($V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $T_a = -40 \text{ to } +85 \text{ }^\circ\text{C}$)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static current consumption * > 350 k gates (65855, 65875) > 150 k gates (65851, 65871) < 150 k gates	I_{DDs}	$V_I = V_{DD}$ or GND		2 1 0.5	300 300 200	μA
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or GND			± 2	μA
Input clamp voltage	V_{IC}	$I_I = 18 \text{ mA}$				V
Output short-circuit current	I_{OS}	$V_O = 0 \text{ V}$			250	mA
Input leakage current						
Normal input	I_I	$V_I = V_{DD}$ or GND		$\pm 10^{-5}$	± 10	μA
with pull-up (50 k Ω)	I_I	$V_I = \text{GND}$	-10	-40	-80	μA
with pull-up (5 k Ω)	I_I	$V_I = \text{GND}$	-135	-350	-640	μA
with pull-down (50 k Ω)	I_I	$V_I = V_{DD}$	30	65	130	μA
Pull-Up Resistor (50 k Ω)	R_{PU}		45	82.5	300.0	k Ω
Pull-Up Resistor (5 k Ω)	R_{Pu}		5.5	9.4	32.1	k Ω
Pull-Down Resistor (50 k Ω)	R_{PD}		27.7	50.8	100.0	k Ω
Low output voltage (3/5 V I/F)	V_{OL}	$I_{OL} = 0 \text{ mA}$			0.1	V
High output voltage (CMOS)	V_{OH}	$I_{OH} = 0 \text{ mA}$ (3 V I/F) (5 V I/F)	$V_{DD} - 0.1$ $V_{DD} - 0.2$			V
Low-level output current (3 V I/F)						
3.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	3.0			mA
6.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	6.0			mA
9.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	9.0			mA
12.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	12.0			mA
18.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	18.0			mA
24.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	24.0			mA
High-level output current (3 V I/F)						
3.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-3.0			mA
6.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-6.0			mA
9.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-9.0			mA
12.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-12.0			mA
18.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-18.0			mA
24.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-24.0			mA
Low-level output current (5 V I/F)						
1.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	1.0			mA
2.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	2.0			mA
3.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	3.0			mA
6.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	6.0			mA
9.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	9.0			mA
12.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	12.0			mA
High-level output current (5 V I/F)						
1.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-3.0			mA
2.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-3.0			mA
3.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-3.0			mA
6.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-6.0			mA
9.0 mA	I_{OH}	$V_{OH} = 2.4 \text{ V}$	-6.0			mA

DC Characteristics ($V_{DD} = 3.0 \text{ V} \pm 10\%$, $T_a = -40 \text{ to } +85 \text{ }^\circ\text{C}$)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static current consumption * > 350 k gates (65855, 65875) > 150 k gates (65851, 65871) < 150 k gates	I_L	$V_I = V_{DD}$ or GND		2 1 0.5	300 300 200	μA
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or GND			± 2	μA
Input clamp voltage	V_{IC}	$I_I = 18 \text{ mA}$				V
Output short-circuit current	I_{OS}	$V_O = 0 \text{ V}$			250	mA
Input leakage current						
Normal input	I_I	$V_I = V_{DD}$ or GND		$\pm 10^{-5}$	± 10	μA
with pull-up (50 kΩ)	I_I	$V_I = \text{GND}$	-45	-100	-320	μA
with pull-up (5 kΩ)	I_I	$V_I = \text{GND}$	-0.35	-1.0	-2.2	mA
with pull-down (50 kΩ)	I_I	$V_I = V_{DD}$	45	100	320	μA
Low output voltage (3/5 V I/F)	V_{OL}	$I_{OL} = 0 \text{ mA}$			0.1	V
High output voltage (CMOS)	V_{OH}	$I_{OH} = 0 \text{ mA}$ (3 V I/F) (5 V I/F)	$V_{DD} - 0.1$ $V_{DD} - 0.2$			V
Low-level output current (3 V I/F)						
3.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	3.0			mA
6.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	6.0			mA
9.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	9.0			mA
12.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	12.0			mA
18.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	18.0			mA
24.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	24.0			mA
High-level output current (3 V I/F)						
3.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-3.0			mA
6.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-6.0			mA
9.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-9.0			mA
12.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-12.0			mA
18.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-18.0			mA
24.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-24.0			mA
Low-level output current (5 V I/F)						
1.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	1.0			mA
2.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	2.0			mA
3.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	3.0			mA
6.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	6.0			mA
9.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	9.0			mA
12.0 mA	I_{OL}	$V_{OL} = 0.4 \text{ V}$	12.0			mA
High-level output current (5 V I/F)						
1.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-3.0			mA
2.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-3.0			mA
3.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-3.0			mA
6.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-6.0			mA
9.0 mA	I_{OH}	$V_{OH} = 2.2 \text{ V}$	-6.0			mA

Note: * The static current consumption increases if an I/O block with on-chip pull-up/down resistor or an oscillator is used.
The "+" and "-" signs added to the current values indicate their direction ('+' means current into, '-' means out of the device).

Packaging

The benefits of NEC's CMOS-8L family are supported by the right choice of packages. The wide range of packages includes thin packages (T-QFP, L-QFP) and QFP with heat-

spreader or Copper-leadframes, to improve the thermal characteristics. New packages like PGA or BGA (Ball Grid Array) with high pin count are continuously under development.

Package Availability

		Master (μPD65...)													
Package	Pitch [mm]	840 860	841 861	842 862	843 863	845 865	846 866	848 868	849 869	850 870	851 871	852 872	853 873	855 875	858 878
100 QFP (FP)	0.50	-	A	A	A	-	-	-	-	A	-	-	-	-	-
120 QFP (FP)	0.50	-	-	-	A	A	A	-	-	-	-	-	-	-	-
144 QFP (FP)	0.50	-	-	-	-	A	A	A	-	-	-	-	-	-	-
160 QFP (FP)	0.50	A	A	A	P	A	A	A	A	A	A	A	-	-	-
176 QFP (FP)	0.50	-	-	-	-	-	-	P	P	P	P	-	-	-	-
208 QFP (FP)	0.50	-	-	A	A	A	A	P	A	P	A	A	A	A	P
240 QFP (FP)	0.50	-	-	-	A	A	A	A	A	A	P	A	A	A	P
272 QFP (FP)	0.50	-	-	-	-	P	P	P	P	P	P	P	P	P	P
304 QFP (FP)	0.50	-	-	-	-	-	-	A	A	P	A	A	A	A	P
256 QFP (FP)	0.40	-	-	-	-	A	A	P	P	P	P	P	P	P	P
160 QFP-Hsp	0.65	-	-	-	-	-	-	-	-	-	A	-	-	-	-
160 QFP-Hsp	0.50	-	-	-	-	-	A	A	A	P	A	A	-	-	-
176 QFP-Hsp	0.50	-	-	-	-	-	-	P	P	P	P	-	-	-	-
208 QFP-Hsp	0.50	-	-	-	-	-	-	-	-	A	A	A	A	A	P
100 T-QFP	0.50	-	P	P	-	-	-	-	-	-	-	-	-	-	-
144 T-QFP	0.50	-	-	-	-	-	-	-	-	-	-	-	-	-	-
160 T-QFP	0.50	-	-	-	-	-	-	-	-	-	-	-	-	-	-
176 T-QFP	0.50	-	-	-	-	-	-	-	-	-	-	-	-	-	-
208 T-QFP	0.50	-	-	-	-	-	-	-	-	-	-	-	-	-	-
144 L-QFP	0.50	-	-	-	-	-	P	P	P	P	P	P	P	P	P
160 L-QFP	0.50	P	P	P	P	P	P	P	P	P	P	P	P	P	P
208 L-QFP	0.50	-	-	P	P	P	P	P	P	P	P	P	P	P	P
72 PGA		-	-	-	-	-	-	-	-	-	-	-	-	-	-
132 PGA		-	-	-	-	-	-	-	-	-	-	-	-	-	-
176 PGA		-	A	-	-	-	-	-	-	-	-	-	-	-	-
208 PGA		-	-	A	A	-	-	-	-	-	-	-	-	-	-
280 PGA		-	-	-	-	-	A	A	A	A	A	A	P	P	P
364 PGA		-	-	-	-	-	-	-	A	A	A	A	A	A	A
528 PGA		-	-	-	-	-	-	-	-	-	-	-	A	A	P
288 B/L PGA		-	-	-	-	-	-	-	-	-	-	-	-	-	-
528 B/L PGA		-	-	-	-	-	-	-	-	-	-	-	A	A	P

Note: FP = Fine Pitch
 T = Thin package (1 mm thick)
 L = Low profile package (1.4 mm thick),
 Hsp = with integrated Heat Spreader
 B/L = Butt Lead (surface mount PGA)
 A = available master package combination
 P = master package combination under development or planned; availability must be confirmed by NEC

Block Library

The functions of the CMOS-8L blocks are designed to be compatible with those of the CMOS-6 and CMOS-8 family. The CMOS-8L family offers a wide variety of advanced blocks, including combination gates, shift registers, adders and counters. In addition, memory blocks such as RAM

and ROM will be provided, and low-power gates are available. The low-power blocks are designed for gate count reduction; the number of cells are fewer than that of the standard block, contributing to lower power consumption and higher efficiency. The signal interface to 5 V logic is supported by special I/O macro blocks.

I/O Buffer

Buffer Type	Options and possible combinations
Input Buffer	Pull-Up 50 kΩ, 5 kΩ / Pull-Down 50 kΩ / Schmitt Trigger Input/ Fail Safe/ High Fanout (Clock Driver) / PCI (3 V / 5 V) / GTL / TTL
Output Buffer, Bidirectional I/O Buffer	Drive Ability: 3, 6, 9, 12, 18, 24 mA (3 V) / 1, 2, 3, 6, 9 mA (5 V) / TTL / Open Drain / Tri-State / Low Noise (Slew rate) / PCI (3 V / 5 V) / GTL

Memory Blocks

Type (Function)	Operation	Bit range	Word range
High density single port RAM	Asynchronous	4 to 40	128 to 4k
High speed single port RAM	Asynchronous	2 to 128	4 to 1k
High speed dual port RAM	Asynchronous	2 to 128	4 to 1k
Standard ROM	Asynchronous	4 to 32	128 to 8k

Block List

Block Name	Description	Block Name	Description
Interface Blocks		Buffers	
F091	H,L level generator	F111	Non-Inverting Buffer (F/O = 10)
F093	Interface block for Oscillator buffer	F112	Non-Inverting Buffer (F/O = 20)
Clock Drivers		F113	Non-Inverting Buffer (F/O = 30)
FCK1	Clock Driver (F/O = 279)	F114	Non-Inverting Buffer (F/O = 40)
FCK2	Clock Driver (F/O = 565)	F118	Non-Inverting Buffer (F/O = 80)
FCK3	Clock Driver (F/O = 864)	Three-State Buffers	
FCK4	Clock Driver (F/O = 1344)	F531	3-state Buffer with EN
FCK5	Clock Driver (F/O = 1440)	F532	3-state Buffer with ENB
Inverters		Delays	
F101	Inverter	F130	Delay Gate
F102	Inverter	F131	Delay Gate
F103	Inverter	F132	Delay Gate
F104	Inverter		
F108	Inverter		

Block Name	Description
NOR Gates	
F202	2-Input NOR
F203	3-Input NOR
F204	4-Input NOR
F205	5-Input NOR
F206	6-Input NOR
F208	8-Input NOR
F222	2-Input NOR (Power)
F223	3-Input NOR (Power)
F224	4-Input NOR (Power)
OR Gates	
F212	2-Input OR
F213	3-Input OR
F214	4-Input OR
F215	5-Input OR
F216	6-Input OR
F232	2-Input OR (Power)
F233	3-Input OR (Power)
F234	4-Input OR (Power)
NAND Gates	
F302	2-Input NAND
F303	3-Input NAND
F304	4-Input NAND
F305	5-Input NAND
F306	6-Input NAND
F308	8-Input NAND
F322	2-Input NAND (Power)
F323	3-Input NAND (Power)
F324	4-Input NAND (Power)
AND Gates	
F312	2-Input AND
F313	3-Input AND
F314	4-Input AND
F315	5-Input AND
F316	6-Input AND
F332	2-Input AND (Power)
F333	3-Input AND (Power)
F334	4-Input AND (Power)
AND-OR Gates	
F421	2-Wide, 1-2-input AND-OR-Inverter
F422	3-Wide, 1-1-2-input AND-OR-Inverter
F423	2-Wide, 1-3-input AND-OR-Inverter
F424	2-Wide, 2-2-input AND-OR-Inverter
F425	3-Wide, 2-2-2-Input AND-OR-Inverter
F426	2-Wide, 3-3-Input AND-OR-Inverter
F429	4-Wide, 2-2-2-Input AND-OR-Inverter
F442	2-Wide, 4-4-Input AND-OR-Inverter
F462	3-Wide, 1-2-3-Input AND-OR-Inverter
OR-AND Gates	
F431	2-Wide, 1-2-Input OR-AND-Inverter
F432	3-Wide, 1-1-2-Input OR-AND-Inverter
F433	2-Wide, 1-3-Input OR-AND-Inverter
F434	2-Wide, 2-2-Input OR-AND-Inverter
F435	2-Wide, 2-3-Input OR-AND-Inverter
F436	2-Wide, 3-3-Input OR-AND-Inverter
F454	4-Wide, 2-2-2-Input OR-AND-Inverter

Block Name	Description
Exclusive OR Functions	
F511	Exclusive-OR
F512	Exclusive-NOR
Adders	
F521	1-bit Full Adder
F523	4-bit Binary Full Adder
F526	Look Ahead Carry Generator
F527	4-bit Full Adder
Decoders	
F561	2 to 4 Decoder
F981	2 to 4 Decoder with ENB
F982	3 to 8 Decoder with ENB
Multiplexers	
F563	Non-inverting 8 to 1 Multiplexer
F564	Non-inverting 4 to 1 Multiplexer
F565	Non-inverting 2 to 1 Multiplexer
F569	8 to 1 Multiplexer with ENB
F570	4 to 1 Multiplexer with ENB
F571	2 to 1 Multiplexer with ENB
F572	Quad 2 to 1 Multiplexer
Parity Generators	
F581	8-bit Odd Parity Generator
F582	8-bit Even Parity Generator
Latches	
F595	RS-Latch
F601	D-Latch
F602	D-Latch with R
F603	D-Latch with RB
F604	D-Latch GB
F605	D-Latch GB with RB
F901	4-bit Latch
F902	8-bit Latch
Flip-Flops	
F596	Synchronous RS-F/F with Set, Reset
F611	D-F/F
F614	D-F/F with S, R
F615	D-F/F with RB
F616	D-F/F with SB
F617	D-F/F with SB, RB
F631	D-F/F CB
F637	D-F/F CB with SB, RB
F641	D-F/F (Buffered Out)
F644	D-F/F with S, R (Buffered Out)
F647	D-F/F with SB, RB (Buffered Out)
F661	D-F/F CB (Buffered Out)
F667	D-F/F CB SB, RB (Buffered Out)
F714	T-F/F with S, R
F717	T-F/F with SB, RB

Block Name	Description
Flip-Flops (Cont.)	
F737	T-F/F TB with SB, RB
F744	T-F/F with S, R (Buffered Out)
F747	T-F/F with SB, RB (Buffered Out)
F767	T-F/F TB with SB, RB (Buffered Out)
F771	JK-F/F (Buffered Out)
F774	JK-F/F with S, R (Buffered Out)
F777	JK-F/F with SB, RB (Buffered Out)
F781	JK-F/F CB (Buffered Out)
F787	JK-F/F CB with SB, RB (Buffered Out)
F791	T-F/F with S, R, TE
F792	T-F/F TB with SB, RB, TEB
F922	4-bit D-F/F with R
F924	4-bit D-F/F
Shift Registers	
F911	4-bit Shift Register with R
F912	4-bit Serial/Parallel Shift Register
F913	4-bit Parallel in Shift Register with RB
F914	4-bit Shift Register
F915	4-bit Shift Register with direct LOADB (Buffered Out)
Counters	
F961	4-bit Sync. Binary Counter with RB (Buffered Out)
F962	4-bit Synchronous Binary Up-Counter with RB
F963	Presetable Synchronous Up/Down Binary Counter (Dual clock, with Clear)
F964	Presetable Synchronous Up/Down Binary Counter
Comparator	
F985	4-bit Magnitude Comparator

Function Blocks - Low Power

Inverter	
L101	Inverter (F/O = 10)
Buffer	
L111	Non-Inverting Buffer (F/O = 10)
NOR Gates	
L202	2-Input NOR
L203	3-Input NOR
L204	4-Input NOR
OR Gates	
L212	2-Input OR
L213	3-Input OR
L214	4-Input OR
NAND Gates	
L302	2-Input NAND
L303	3-Input NAND
L304	4-Input NAND
L305	5-Input NAND
L306	6-Input NAND
AND Gates	
L312	2-Input AND
L313	3-Input AND
L314	4-Input AND

Block Name	Description
AND-OR Gates	
L421	2-Wide, 1-2-input AND-OR-Inverter
L422	3-Wide, 1-1-2-input AND-OR-Inverter
L423	2-Wide, 1-3-input AND-OR-Inverter
L424	2-Wide, 2-2-input AND-OR-Inverter
L425	3-Wide, 2-2-2-Input AND-OR-Inverter
L426	2-Wide, 3-3-Input AND-OR-Inverter
L429	4-Wide, 2-2-2-2-Input AND-OR-Inverter
L442	2-Wide, 4-4-Input AND-OR-Inverter
L462	3-Wide, 1-2-3-Input AND-OR-Inverter
OR-AND Gates	
L431	2-Wide, 1-2-Input OR-AND-Inverter
L432	3-Wide, 1-1-2-Input OR-AND-Inverter
L433	2-Wide, 1-3-Input OR-AND-Inverter
L434	2-Wide, 2-2-Input OR-AND-Inverter
L435	2-Wide, 2-3-Input OR-AND-Inverter
L436	2-Wide, 3-3-Input OR-AND-Inverter
L454	4-Wide, 2-2-2-2-Input OR-AND-Inverter
Exclusive OR Functions	
L511	Exclusive-OR
L512	Exclusive-NOR
Decoders	
L561	2 to 4 Decoder
L981	2 to 4 Decoder with ENB
L982	3 to 8 Decoder with ENB
Multiplexers	
L571	2 to 1 Multiplexer with ENB
L572	Quad 2 to 1 Multiplexer
Latches	
L601	D-Latch
L602	D-Latch with R
L603	D-Latch with RB
L604	D-Latch GB
L605	D-Latch GB with RB
L901	4-bit Latch
L902	8-bit Latch
Flip-Flops	
L611	D-F/F
L614	D-F/F with S, R
L617	D-F/F with SB, RB
L631	D-F/F CB
L637	D-F/F CB with SB, RB
L714	T-F/F with S, R
L717	T-F/F with SB, RB
L737	T-F/F TB with SB, RB
L922	4-bit D-F/F with R
L924	4-bit D-F/F
Shift Registers	
L911	4-bit Shift Register with R
L912	4-bit Serial/Parallel Shift Register
L913	4-bit Parallel in Shift Register with RB
L914	4-bit Shift Register

Block

Name	Description
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Scan Path Blocks

Flip-Flops

S000	D-F/F with S, R (Scan Path)
S002	D-F/F (Scan Path)
S050	D-F/F with S, R, H (Scan Path)
S052	D-F/F with H (Scan Path)
S100	JK-F/F with S, R (Scan Path)
S102	JK-F/F (Scan Path)
S150	JK-F/F with S, R, H (Scan Path)
S152	JK-F/F with H (Scan Path)

Latches

S201	D-Latch with R (Scan Path)
S202	D-Latch (Scan Path)
S301	D-Latch with R (ATG)
S302	D-Latch (ATG)

Multiplexer

S999	2 to 1 Data Selector (Scan Path)
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Further Publications

This data sheet contains a reduced set of information and operational data for the CMOS-8 gate array family. Additional information is available in NEC's CMOS-8 Design Manual and CMOS-8 Block Library.

Please contact your local NEC Design Centre for further informations.

Notes: