

# CB-10VX family

## Product Letter

# 0.25 $\mu\text{m}$

## CB-10VX Cell-based CMOS ICs

### Description

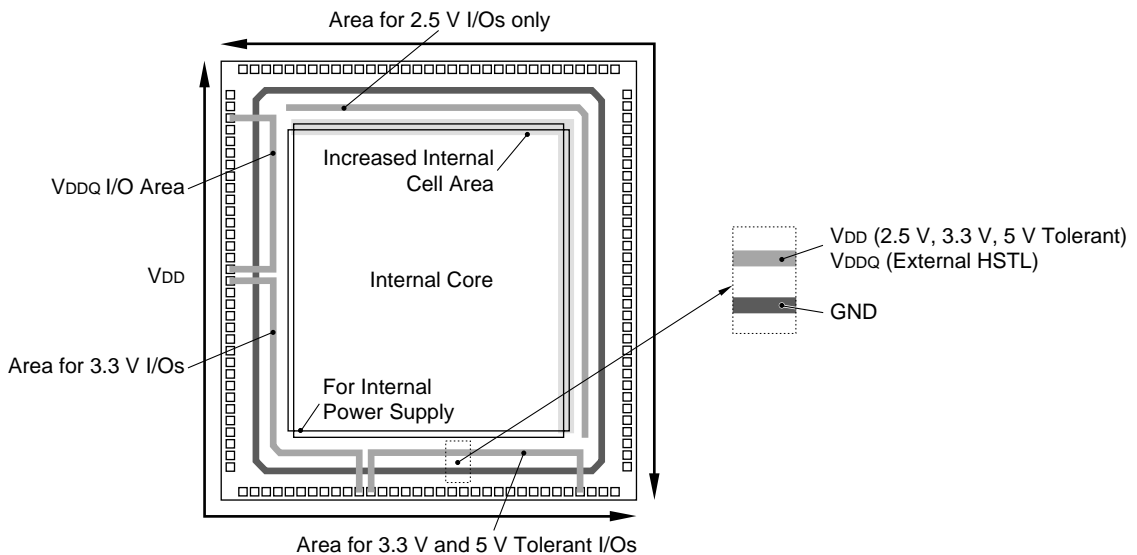
NEC's quarter-micron technology incorporates high performance cell-based ASICs for high/mid-end applications requiring high speeds, high integration density and low power consumption.

The cell-based approach allows the most effective realisation of true "system on a chip" applications. These may be composed of user-defined logic, high density multi-port memory, cores such as CPUs, DSPs or intelligent peripherals and analog-functions.

### Features

- 0.25  $\mu\text{m}$  (drawn, 0.18  $\mu\text{m}$  effective) Ti-Silicide CMOS process
- Extensive support of state-of-the-art cores and interfaces
- Available gate counts from 597k to 21.3 million gates
- Supports 1.8 V and 2.5 V core voltages
- Significant low power dissipation of 0.024  $\mu\text{W}/\text{MHz}/\text{gate}$  @1.8 V
- Multi-oxide process enables full-swing 2.5 V, 3.3 V and 5 V tolerant interfaces
- Flexible I/O structure supports LVDS, HSTL, GTL+, PCI, ...
- Advanced packages like Tape BGA, Advanced BGA, Flip-Chip BGA, ...

### Chip Design Concept



System @ IC  
Solutions on a Chip

# NEC

## Product Outline

Master Name	μPD85xxx (27 die steps)	
Available Gate Count	597k to 21349k	
Number of pads	300 to 2016	
Toggle Frequency (Type)	1.8 GHz	
Delay Time	Internal	38.8 ps (F/O=2, l=0 mm, V <sub>DD</sub> =2.5 V)
	Input	74.8 ps (F/O=2, l=0)
	Output	1.264 ns (I <sub>ol</sub> =9 mA, C <sub>i</sub> =50 pF)
Consumed Power	0.048 μW/MHz/gate @V <sub>DD</sub> =2.5 V	
Power Supply Voltage	2.5 V & 1.8 V	
Operating Temperature	-40 to +85°C	
Interface Level	2.5 V/3.3 V CMOS level, 5 V tolerant LVDS, LVTTTL, GTL+, HSTL, PCI, pECL, PCI, SSTL	
Technology	Standard cell 0.25 μm (0.18 μm effective) silicon gate CMOS: 3, 4, 5 or 6 Al-metal layers (the 6 <sup>th</sup> layer is solely used for Bump Pads)	

## Interfacing

### I/O Region

The CB-10VX interface structure provides a variety of interface options. A wide range of different interface blocks – 334 blocks in total – allows easy integration in 2.5 Volt and 3.3 Volt systems.

Thanks to the multi-oxide process, full-swing 2.5 Volt and 3.3 Volt I/Os together with 5 Volt tolerant buffers are available. Using the power rail structure shown in the front page figure, different voltage level buffers can be mixed. The 2.5 Volt and 3.3 Volt buffers have different heights and therefore need different space in the I/O area. In case of pure 2.5 Volt I/Os – as an example – the additional power rail for 3.3 Volt I/Os can be omitted. In this case, the remaining area can also be used for internal cells, resulting in an optimised and thus cost effective die size.

### High-speed interfaces

CB-10VX supports a wide set of high-speed interface macros with very low power consumption, covering the full range from 150 Mbps up to 860 Mbps. Receivers include per-channel clock-data recovery with an arbitrary number of channels, limited only by die size constrains. Possible interfaces are pECL, LVDS or low power LVDS.

### HSTL/PCI

For designs using HSTL or PCI I/O blocks, the above described power rail structure supports the additional required supply voltage of 1.4 Volt (V<sub>DD0</sub> for HSTL) or 3.3 Volt (for PCI) in special power rails and pin assignment.

## Features

### Architecture

The CB-10VX family takes advantage of NEC's perfected Titanium Silicide (Ti-Si) process that leads to a higher integration density combined with improved speed performance. The chip layout is done using between three and five metal layers (Al), whereas the sixth layer is used for wiring the area-pads in case of high pin-count packages. As the CB-10VX ASIC follows a cell-based approach, it offers highest flexibility concerning power routing, split power supply lines and other customer specific requirements.

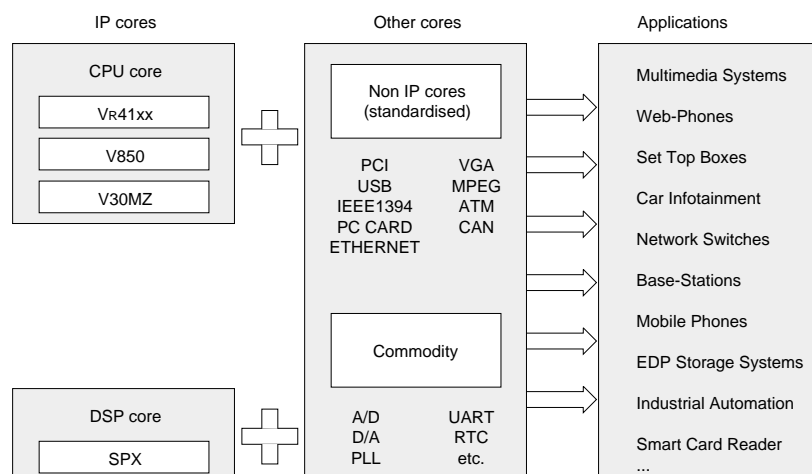
### Memories

Various kinds of memory macros are available for CB-10VX. The cell-based type memory blocks are generated based on advanced memory-compiler tools and thus ensure highest flexibility according to customer requirements. Single- and dual port synchronous memories in high-density and high-speed configurations together with asynchronous register files are supported.

Type (Function)	Maximum Size (Words x Bits)
High Density Single Port RAM	32kw x 72b
High Speed Dual Port RAM	4kw x 64b
High Density Dual Port RAM	4kw x 64b
High Density ROM	64kw x 64b
High Speed ROM	8kw x 64b
Multi Port Register Files	512w x 72b

### Macros

The high integration density of up to 21.3 million available gates offered by CB-10VX builds the foundation for complete system on a chip integration. This trend is driven by NEC with a strong support for high complex macro blocks which in many cases represent the functionality of well known state-of-the-art standard devices.



# 0.25 $\mu\text{m}$

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### Further Publications

This product letter contains preliminary specifications and operational data for the CB-10VX family. Additional information is available in NEC's CB-10VX Design Manual, Block Library and other related documents.

Please contact your local NEC Design Center for further information; see the back of this product letter for locations and telephone numbers.

For further information on NEC's ASICs or other NEC products visit our European website at [www.nec.de](http://www.nec.de)

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