SoC Technology

Product Letter

0.13 µm

CB-12 Cell-based CMOS IC

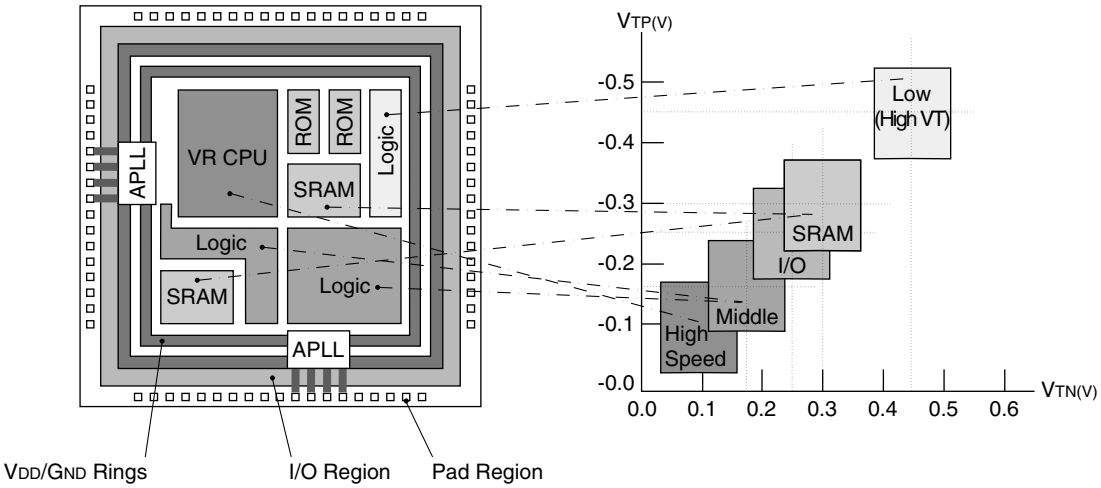
Description

Featuring the selection of three different transistor characteristics on the same chip for achieving the optimum combination of high performance, effective use of area, extreme low power consumption, CB-12 is targeted to enable the implementation of System-on-Chip (SoC) for wide range of application such as telecomm, network, consumer, automotive, industrial. To meet the challenge of both complex system-level design and fast time-to-market, NEC is supplying total design support for hardware, software design and system integration.

Features

- 0.13 µm (drawn, 0.11 µm effective) Cobalt Salicide CMOS process
- Three transistor characteristics (low power, standard, high performance) selectable on the same chip
- Up to 8 Metal layers
- Up to 32 million available gates
- System frequency: up to 450 MHz
- Core voltage 1.5 V with optimized architecture
- Extreme low power dissipation down to 13 nW/MHz/gate
- I/O voltage : 2.5 V, 3.3 V, 5 V tolerant
- Flexible I/O structure supports LVTTL, GTL+ ,HSTL, SSTL, PCI, USB, AGP, LVDS, pECL
- Various package types available: QFP, FPBGA, TBGA, ABGA, PBGA, FCBGA (up to 2700 pins)

Chip Design Concept



System@IC
Solutions on a Chip

NEC

Product Outline

Master Name		µPD80xxx (44 die steps)
Metal Layer		up to 8
Available Gate Count (max.)		32 million
Number of Pads		up to 2700 with FCBGA
Toggle Frequency (Standard)		5.4 GHz
Gate Delay (FO = 2, 2NAND, I = 0)	Standard	21.2 ps
	Low Power	31.7 ps
Gate Power Consumption		13 nW/MHz/gate
Power Supply Voltage		1.5 V ± 0.15 V
Operating Temperature		-40 to +85°C
Interface Level		2.5 V/3.3 V CMOS, LVTTL
Technology		Standard cell 0.13 µm (0.11 µm effective) silicon gate CMOS; up to 8 metal layers

Features

Architecture

Manufactured with NEC's advanced Cobalt-Salicide process, the CB-12 SoC technology offers the choice of three transistor characteristics for enabling an optimum configuration of performance/low power/high-integration targeted area partitioning on the same chip. The selectable Ion/Ioff switching characteristics, which can be used e.g. to achieve an optimum speed for CPUs and low power consumption for user logic, enables the implementation of a high performance application requiring a minimum of electrical power.

Interfacing

The CB-12 I/O structure enables the broad variety of interfacing support. I/O voltage of 2.5 V, 3.3 V will be supported as well as 5 V tolerant buffers and PCI buffers. GTL+, HSTL, SSTL, AGP, USB, LVDS, pECL standard will be supported for high-speed interfacing. Pad pitches of 50 µm and 80 µm support a broad range of package selection like QFP, FPBGA, TBGA, ABGA, PBGA, FCBGA with up to 2700 pins to meet all kind of appliances.

System-on-Chip

Leading edge system integration implies a total solution with both software / hardware design and integration.

System-on-Chip Integration

The rich portfolio of NEC's ASIC pre-verified mega-macros increases the hardware design efficiency of a typical System-on-Chip project, which requires processor/DSP cores, memories, peripherals and analog functions. The CPU architecture selection ranges from MIPS architecture to NEC's V850 and ARM946, all kind of high-speed and low-speed bus peripherals like memory controllers, system controllers and communication function are supported. To enable the easy software integration NEC's CPU cores are supported by a number of industry-standard software development tools including OS, debuggers and emulators as well as a broad portfolio of firmware for various appliances. For the smooth concurrent design & integration, NEC offers the support for industry leading hardware/ software co-verification tools

Test

For testing complex System-on-chip, a new approach of block level testing is required which must ensure sufficient testing with high fault coverage in a reasonable engineering time. In addition to conventional Scan test methodology NEC will support NEC's TestBus concept and Built-in-Self-Test (BIST) for memory macros.

System-on-Chip Design Support

For meeting the challenge of a very deep submicron design and the system-level integration NEC takes two leading edge design approach.

- System-level design including hardware/software co-simulation/co-verification on a block–based system design approach
- NEC's sophisticated design framework OpenCAD™ including physical floor planning, timing driven layout, hierarchical design.

Further Publications

This product letter contains preliminary specifications and operational data for the CB-12 ASIC family. Additional information is available in NEC's CB-12 Design Manual, Block Library and other related documents.

Please contact your local NEC Design Center for further information; see the back of this product letter for locations and telephone numbers.

For further information on NEC's ASICs or other NEC products visit our European website at **www.ee.nec.de**

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