

## EA-C10 2.5 Volt 0.25-Micron CMOS Embedded Array PRELIMINARY

### Description

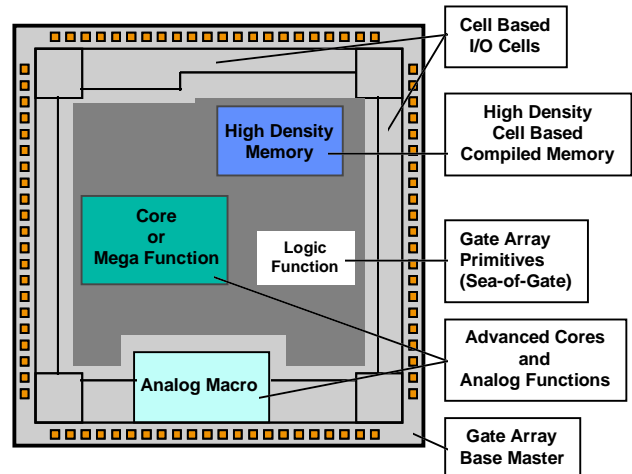
The high speed 0.25  $\mu\text{m}$  (0.18  $\mu\text{m}$  eff.) EA-C10 embedded array family offers support for embedded high density macros combined with a short TAT of a gate array resulting in a time-to-market advantage. NEC combines high performance CMOS gate array primitives with diffused embedded mega functions such as RAM, ROM, CPUs or DSP cores.

EA-C10 uses a cell based I/O structure. This allows a flexible adaptation to the system requirements. State-of-the-art interface macros for high speed or special signalling systems are also supported - such as PCI, HSTL, GTL+ and IEEE1394. Analog functions like DACs or ADCs can be incorporated within the I/O area.

### Process

EA-C10 ASICs are manufactured in NEC's advanced titanium-silicide (Ti-Si) process. The chip layout is done using between three and five metal layers (Al). As the EA-C10 ASIC family follows basically a gate array approach, it offers short turn-around times for silicon processing and lower development costs compared to cell-based ASICs. The TAT can be kept short by pre-diffusion of the embedded area which is used in the design.

**Figure 1. Embedded Array Core Integration**



### Applications

The EA-C10 family is ideal for applications where high density is mandatory and a short time-to-market is required. For example, RAM dominated designs can be realised with reduced die size and a reasonable TAT. EA-C10 is well suited in terms of re-work, because the logic function portion of the design is realised with gate array primitives which are defined just by the final wiring masks. Typical applications include engineering workstations, telecommunications systems, advanced graphics or low power applications where very high performance is required. Package requirements are supported by a wide range of different package types.

**Table 1. EA-C10 Series Features and Benefits**

EA-C10 Series Features	EA-C10 Series Benefits
• 0.25 $\mu\text{m}$ (drawn, 0.18 $\mu\text{m}$ eff.) Ti-Silicide CMOS process	⇒ Ultra high density cell structure at high performance
• Advanced embedded array architecture	⇒ Fast TAT and high integration of embedded mega functions
• Available gate counts from 206K to 7 million gates	⇒ Support for a wide range of high complex systems
• Optimised 2.5 V architecture (operates down to 1.8 V)	⇒ Highest speed at ultra low power consumption
• Significant low power dissipation of 0.14 $\mu\text{W}/\text{MHz}/\text{gate}$	⇒ New application possibilities and new system solutions
• Ultra high pin count by using 40 $\mu\text{m}$ pad pitch	⇒ Increases the I/O density at smaller die sizes
• Special power rail structure, multi-oxide process	⇒ Mixed 2.5 V / true 3.3 V I/O for full system compatibility
• Cell based I/O structure incl. LVDS, HSTL, GTL+, PCI, ...	⇒ Flexible adaptation to system requirements
• Embedding of analog macros incl. DACs, ADCs, ...	⇒ Extends the application to analog systems
• Advanced packages like TapeBGA, Flip Chip+BGA, ...	⇒ Delivers cost-effective and state-of-the-art system solutions
• NEC's OpenCAD <sup>®</sup> design environment	⇒ Standard commercial EDA sign-off for flexible design flow

**Table 2. Product Outline**

Master ( $\mu$ PD69..) 3 Layer	..101	..102	..103	..104	..105	..107	..109	..111	..112	..113	..114	..115
Master ( $\mu$ PD69..) 4 Layer	..121	..122	..123	..124	..125	..127	..129	..131	..132	..133	..134	..135
Master ( $\mu$ PD69..) 5 Layer*	..141	..142	..143	..144	..145	..147	..149	..151	..152	..153	..154	..155
Available Gate Count (raw)	206k	338k	497k	690k	1041k	1611k	2127k	2509k	3137k	3597k	4089k	6937k
Number of pads <sup>(40 <math>\mu</math>m pitch)</sup>	348	444	540	636	780	972	1116	1212	1356	1452	1548	2016
Utilisation	80% / 85% for 3 / 4 metal layers											
Toggle Frequency (Typ.)	2.0 GHz											
Delay time	internal	59 ps (F/O = 1, l = 0.5 mm); 147.5 ps (F/O = 2, l = typ. average length) <sup>(F322)</sup>										
	input	79.7 ps (F/O = 2, l = 0 mm) <sup>(F101)</sup>										
	output	1.363 ns ( $C_L = 50$ pF) <sup>(F002)</sup>										
Consumed Power	internal	0.14 $\mu$ W/MHz/gate (2.5 V)										
	input	1.66 $\mu$ W/MHz (F/O = 2, l = 0 mm)										
	output	167 $\mu$ W/MHz ( $C_L = 15$ pF)										
Power supply voltage	2.5 V $\pm$ 0.2 V (operation down to 1.8 V possible)											
Operating temperature	-40 to +85°C											
Interface level	2.5 V / 3.3 V CMOS level, LVTTTL level, GTL+, HSTL, PCI, pECL											
Technology	Sea-of-Gates 0.25 $\mu$ m (0.18 $\mu$ m effective) silicon gate CMOS, diffused embedded macros; 3,4 or 5* Al-metal layers											

(Note \*: 5 metal layer used for flip chip.)

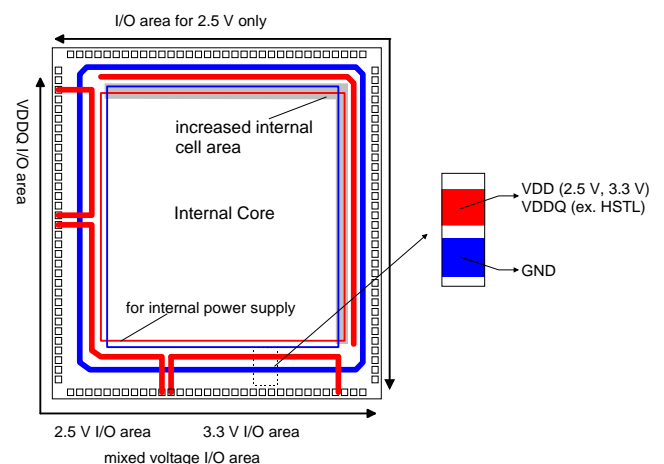
## Interface Macro Support

The EA-C10 interface area is realised by using cell based structures. This provides a variety of interface options. A wide range of different interface blocks allows easy integration in 2.5 Volt and 3.3 Volt systems.

For special applications a set of high-speed I/O buffer types is available. This includes 3.3 V PCI cells for 66 MHz applications, GTL (Gunning Transceiver Logic) I/O cells, HSTL (class 1,2,3,4) interface cells and pseudo ECL (pECL) buffers. These high speed buffers are available for special applications. Table 3 summarises the available interface options.

### 2.5 Volt / 3.3 Volt Mixed I/O Interfacing.

Although EA-C10 is a 2.5 Volt optimised technology with thin gate oxide, NEC offers 3.3 Volt compatible I/O interfacing. The full swing 3.3 Volt interfacing can be achieved through a multi-oxide process in the I/O area. The buffers for 2.5 Volt / 3.3 Volt interface level can be mixed. This is supported by the special power rail structure shown in figure 2.

**Figure 2: Example for Power Rail Option**


**HSTL / PCI Interfacing.** For designs using HSTL or PCI I/O blocks, the power rail structure described above supports the additional supply voltage of 1.4 Volt ( $V_{DDQ}$  for HSTL) or 3.3 Volt (for PCI) in different power rails and pin assignment.

**Table 3. EA-C10 I/O Buffer Types**

Buffer Type	Options and possible combinations
Standard I/O Interface Buffers	Pull-Up 50 kΩ, 5 kΩ / Pull-Down 50 kΩ Schmitt Trigger Input Fail Safe CMOS / LVTTTL Level  Output Buffers: Open Drain Tri-State Low Noise (Slew rate controlled)  Driveability: 3, 6, 9, 12 mA (3.3 V interface) 3, 6, 9, 12, 18, 24 mA / 1 slot (2.5 V interface)
High Speed I/O Buffers	PCI (3 V, up to 64 bit / 66 MHz ) GTL / GTL+ pECL HSTL SSTL LVDS* AGP (66 MHz, 133 MHz) IEEE1394* USB*

Note: \*Under development. Please check the availability of the advanced interfaces with your nearest NEC design centre.

## Block Library Support

The functions of the EA-C10 blocks are designed to be backward compatible with previous families. Thus, an easy migration from previous designs is possible. The library is fully compatible with CMOS-10, the 0.25 μm gate array family.

The library offers a wide variety of advanced blocks, including combinational gates, shift registers, adders and counters. In addition, low-power gates are available. The low-power blocks are designed for usage in case of lower drive requirements. The usage of these blocks results in an overall size reduction because low power blocks are using fewer area than standard blocks.

## Macro Library Support

The embedded array approach allows the combination of high density integration at a reasonable turn-around-time equal to gate arrays. Mega functions and memory blocks such as RAM and ROM can be embedded into the sea-of-gate area within the EA-C10 base master. The area used for the mega functions is defined by a pre-diffusion. The logical function is created by the final metalisation masks. This enables the usage of a gate array master and the whole set of macros which are available in the cell based technology CB-C10.

**Memory Macros.** Of course various kinds of memory macros are available for EA-C10. Customer can select either gate array type memory (asynchronous soft macro, using gate array cells) or cell based type (compiled hard macro) offering a higher density and faster access.

Cell based type memory blocks are generated based on advanced memory-compiler tools and thus ensure highest flexibility according to customer requirements. The available memory types are described in Table 4.

**Table 4. EA-C10 Memory Blocks**

Type ( Function )	Realisation	Mode
RAM (gate array type):		
High speed single port	Soft-Macro	Asyn.
High speed dual port	Soft-Macro	Asyn.
ROM (cell based type):		
Standard	Compiled Hard	Syn.
RAM (cell based type):		
High density single port	Compiled Hard	Syn.
High density dual port	Compiled Hard	Syn.
High speed single port	Compiled Hard	Syn.
High speed dual port	Compiled Hard	Syn.
Super high speed single port	Compiled Hard	Syn.

All memory macros can be combined with a built-in self test (BIST) macro for easy and high performance production testing.

**Analog Macros.** A variety of A/D and D/A converters will be available for analog applications. Analog to digital converters (ADCs) are under development with a bit resolution in the range of 7 bit to 12 bit and a frequency of 100 kHz (for general purpose) up to 30 MHz. Digital to analog converters (DACs)

will also be developed for 7 bit to 12 bit and a frequency of 100 kHz to 220 MHz for high speed conversion.

**Mega Macros.** NEC offer a huge set of mega macros and cores to cope with today's system requirements. The table below shows a subset of the macro portfolio.

**Table 5. EA-C10 Mega Macro Library (subset listing)**

Type	Description	Type	Description
CPU	V30xx: 16 bit microprocessor (several derivatives)	I/F Periph.	71055: progr. parallel interface (3x 8bit)
CPU	70008: 8 bit Z80 microprocessor	I/F Periph.	71059: interrupt controller unit
CPU	V8xx: 32 bit RISC microcontroller (several derivatives)	I/F Periph.	ATM (25 MHz, 155 MHz)
CPU	ARM7TDMI	I/F Periph.	CODEC (Modem, Voice)
CPU	VR4xxx: 64 bit RISC microcontroller (several derivatives)	I/F Periph.	Ethernet 10/100 Base, PHY/MAC
Datapath	High-Speed Multiplier/Accumulator	I/F Periph.	IEEE 1284: Bidirectional Centronics
DSP	OAK: Digital Signal Processor	I/F Periph.	IEEE1394: High speed serial bus
DSP	PINE: Digital Signal Processor	I/F Periph.	MPEG2 Decoder
DSP	SPX: Digital Signal Processor	I/F Periph.	PCI Controller
I/F Periph.	16550: UART with FIFO and 16450 mode	I/F Periph.	RAC: RAMBUS ASIC Cell
I/F Periph.	4993: 8 bit parallel I/O real-time clock	I/F Periph.	USB: Universal Serial Bus Interface
I/F Periph.	71037: DMA Controller	DPLL	Digital PLL (up to 250 MHz)
I/F Periph.	71051: USART, 300kBit/s, full duplex	APLL	Analog PLL (up to 500 MHz)
I/F Periph.	71054: progr. timer/counter		

## Packaging

The advanced pad pitch of 40  $\mu\text{m}$  allows high pin count applications and gives a significant benefit for pad-limited designs. CB-C10 - the new high performance cell-based ASIC family - is supported by a variety of advanced packages. For lower pin counts (up to 376 pins) the standard QFP is available including heatspreader package type to improve the thermal characteristics.

Alternatively, plastic BGAs or tape BGAs in a wide range of ball counts from 256 to 696 balls can help to cope with high complex system requirements by providing excellent electrical and thermal characteristics.

NEC expands the package library continuously with new advanced packages. For high performance applications with high pin counts, the 2-layer Tape BGA with enhanced electrical characteristics can be a solution. Applications which require ultra dense packages can be realised with the Flip Chip package. This can also be used for Multi Chip Module (MCM) structures, where die mounting was previously necessary.

## CAD Support

NEC takes up the challenges of the new ultra high density 0.25  $\mu\text{m}$  technology by using a close relationship with leading CAE vendors to fulfil the design requirements during the whole design flow.

Fully supported by NEC's sophisticated OpenCAD<sup>®</sup> design framework, EA-C10 maximises design quality and flexibility while minimising ASIC design time.

NEC's OpenCAD<sup>®</sup> system allows designers to combine the CAE industry's most popular third-party design tools with proprietary NEC tools, including advanced floorplanner, clock tree synthesis tools, automatic test pattern generation (ATPG), full timing simulation, accelerated fault grading and advanced place and route algorithms. The latest OpenCAD<sup>®</sup> system is open for sign-off using standard EDA tools. NEC offers RTL- and STA-sign-off procedures to shorten the ASIC design cycle of high complexity designs.

**Support of High Speed Systems.** High-speed systems require tight control of clock skew on the chip and between devices on a printed circuit board. EA-C10 provides two features to control clock skew: the Digital PLL (DPLL) working at frequencies up to 250 MHz for chip-to-chip skew minimisation and Clock Tree Synthesis (CTS). CTS - supported by an NEC proprietary design tool - is used for clock skew management through the automatic insertion of a balanced buffer tree. The clock tree insertion method minimises large capacitive trunks and is especially useful with the hierarchical, synthesised design style being used for high integration devices. RC values for actual net lengths of the clock tree are used for back annotation after place and route. A skew as low as  $\pm 60$  ps can be achieved.

**Accurate Design Verification.** Non-linear timing calculation is a very important requirement of the high density deep sub-micron ASIC designs. NEC makes use of the increased accuracy delivered by the non linear table lookup delay calculation methodology and offers consistent wire load models to ensure a high accuracy of the design verification.

**Design Rule Check.** A comprehensive design rule check (DRC) program reports design rule violations as well as chip utilisation statistics for the design netlist. The generated report contains such information as net count, total pin count, gate count, and utilisation figures.

**Layout.** During design synthesis, wire load models are used to get delay estimations in a very early state of the design flow. In general, there's no need for customers to perform the floorplanning to meet the required timing. During layout, enhanced in-place optimisation (IPO) features of the layout tools and engineering change order (ECO) capabilities of the synthesis tools are used to optimise critical timing paths defined by the given timing constraints. This feature can reduce the total design time.

## Test Support

The EA-C10 family supports automatic test generation through a scan test methodology. It includes internal scan, boundary scan (JTAG) and built-in-self-test (BIST) architecture for easy and high performance production RAM testing. This allows higher fault coverage, easier testing and faster development time.

Test of embedded mega macros is supported from NEC's testbus concept, which allows the use of predefined test pattern sets for integrated core macros.

## Further Publications

This product letter contains preliminary specifications and operational data for the EA-C10 embedded array family. Additional information is available in NEC's EA-C10 Design Manual, Block Library and other related documents. Please refer also to the CMOS-10 and CB-C10 product letters to get more information to the 0.25  $\mu\text{m}$  gate array and cell based ASIC products.

Please contact your local NEC Design Centre for further information; see the back of this product letter for locations and telephone numbers.

## Absolute Maximum Ratings

Power supply voltage, $V_{DD}$	3.6 V
Input voltage, $V_I$	
2.5 V input buffer	3.6 V
3.3 V input buffer	4.6 V
Output voltage, $V_O$	
2.5 V buffer	3.6 V
3.3 V buffer	4.6 V
Latch-up current, $I_{LATCH}$	1 A
Operating temperature, $T_{OPT}$	-40 to +85°C
Storage temperature, $T_{STG}$	-65 to +150°C

## Input / Output Capacitance

$V_{DD}=V_I=0$  V;  $f=1$  MHz

Terminal	Symbol	Typ	Max	Unit
Input	$C_{IN}$	4	6	pF
Output	$C_{OUT}$	4	6	pF
I/O	$C_{I/O}$	4	6	pF

Note:(1) Values do not include package pin capacitance.

## Power Consumption

Description	Limits	Unit
Internal Cell (@ 2.5 V supply voltage, loaded)	0.14	$\mu$ W/MHz
Input block (FI01, F/O=2, L=0)	1.66	$\mu$ W/MHz
Output block (F002 @ 15 pF)	167	$\mu$ W/MHz

## Recommended Operating Conditions

Parameter	Symbol	2.5V Buffer		3.3V Buffer		3.3V PCI		Unit
		Min	Max	Min	Max	Min	Max	
Power supply voltage	$V_{DD}$	2.3	2.7	3.0	3.6	3.0	3.6	V
Junction temperature	$T_J$	-40	+125	-40	+125	-40	+125	°C
Low-level input voltage	$V_{IL}$	-0.3	0.7	-0.5	$0.3 V_{DD}$	-0.5	$0.3 V_{DD}$	V
High-level input voltage	$V_{IH}$	1.7	$V_{DD} + 0.3$	$0.5 V_{DD}$	$V_{DD} + 0.5$	$0.5 V_{DD}$	$V_{DD} + 0.5$	V
Input rise or fall time	$t_R, t_F$	0	200	0	200	0	200	ns
Input rise or fall time, Schmitt	$t_{R, t_F}$	0	10	0	10	0	10	ms

## AC Characteristics

$V_{DD} = 2.5$  V  $\pm$  0.2 V;  $T_J = 0$  to +125°C

Parameter	Symbol	Best	Typ	Worst	Unit	Conditions
Toggle frequency	$f_{TOG}$	2.8	2.0	1.1	GHz	D-F/F; F/O = 1
Delay time						
2-input Power - NAND (F322)	$t_{PD}$	30.5	41.1	67.5	ps	F/O = 2; L = 0 mm
	$t_{PD}$	43.6	59.0	96.4	ps	F/O = 1; L = 0.5 mm
Flip-flop (F611)	$t_{PD}$	200	278	465	ps	F/O = 1; L = 0 mm
	$t_{PD}$	242	336	558	ps	F/O = 2; L = 0.5 mm
	$t_{SETUP}$	170	220	340	ps	—
	$t_{HOLD}$	60	50	50	ps	—
Input buffer (FI01)	$t_{PD}$	77.8	103	188	ps	F/O = 1; L = 0.5 mm
	$t_{PD}$	63.0	79.7	144	ps	F/O = 2; L = 0 mm
Input buffer (3.3 V) *	$t_{PD}$	190	286	510	ps	F/O = 1; L = 0.5 mm
	$t_{PD}$	173	255	451	ps	F/O = 2; L = 0 mm
Output buffer (12 mA) 2.5V	$t_{PD}$	287	439	779	ps	$C_L = 0$ pF
Output buffer (12 mA) 2.5V	$t_{PD}$	932	1363	2312	ps	$C_L = 50$ pF
Output buffer (12 mA) 3.3V *	$t_{PD}$	457	659	1192	ps	$C_L = 0$ pF
Output buffer (12 mA) 3.3V *	$t_{PD}$	1386	2115	3554	ps	$C_L = 50$ pF
Output rise time (12 mA)	$t_R$	0.73	1.03	1.83	ns	$C_L = 15$ pF; 10-90%
Output fall time (12 mA)	$t_F$	0.75	0.93	1.55	ns	$C_L = 15$ pF; 10-90%

Note \*: including delay of level shifter circuit

## DC Characteristics

$V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$ ;  $T_j = 0 \text{ to } +125^\circ \text{ C}$

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current						
<= 2000K gates	$I_{DDS}$		4.0	800	$\mu\text{A}$	$V_I = V_{DD}$ or GND
> 2000K gates	$I_{DDS}$		7.0	1400	$\mu\text{A}$	$V_I = V_{DD}$ or GND
Off-state output leakage current						
2.5V output	$I_{OZ}$			$\pm 10$	$\mu\text{A}$	$V_O = V_{DD}$ or GND
3.3V output	$I_{OZ}$			$\pm 10$	$\mu\text{A}$	$V_O = V_{DD}$ or GND
Output sink current with pull-up ( $V_O = 2.5\text{V}$ )	$I_R$				$\mu\text{A}$	$V_{PU} = 3.3 \text{ V}$ , $R_{PU} = 2\text{k}\Omega$
Output sink short circuit current	$I_{OS}$			-250	$\text{mA}$	$V_O = \text{GND}$
Input leakage current						
Regular	$I_I$		$\pm 10^{-4}$	$\pm 10$	$\mu\text{A}$	$V_I = V_{DD}$ or GND
50 k $\Omega$ pull-up	$I_I$		T.B.D.		$\mu\text{A}$	$V_I = \text{GND}$
5 k $\Omega$ pull-up	$I_I$		T.B.D.		$\text{mA}$	$V_I = \text{GND}$
50 k $\Omega$ pull-down	$I_I$		T.B.D.		$\mu\text{A}$	$V_I = V_{DD}$
Pull-up resistor						
50 k $\Omega$ pull-up	$R_{PU}$		T.B.D.		$\text{k}\Omega$	
5 k $\Omega$ pull-up	$R_{PU}$		T.B.D.		$\text{k}\Omega$	
50 k $\Omega$ pull-down	$R_{PD}$		T.B.D.		$\text{k}\Omega$	
Low-level output current						
2.5V buffers						
3 mA	$I_{OL}$	11.0	8.8	5.2	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
6 mA	$I_{OL}$	22.3	17.6	11.5	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
9 mA	$I_{OL}$	33.5	26.5	15.8	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
12 mA	$I_{OL}$	44.5	35.3	21.2	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
18 mA	$I_{OL}$	66.7	52.9	31.7	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
24 mA	$I_{OL}$	88.7	70.5	42.3	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
3.3V buffers (Full Swing)						
3 mA	$I_{OL}$	20.5	14.5	8.3	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
6 mA	$I_{OL}$	30.3	21.7	12.5	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
9 mA	$I_{OL}$	40.5	29.0	16.7	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
12 mA	$I_{OL}$	46.8	36.0	20.8	$\text{mA}$	$V_{OL} = 0.4 \text{ V}$
Low-level output voltage						
2.5V buffers	$V_{OL}$			0.1	$\text{V}$	$I_{OL} = 0 \text{ mA}$
3.3V buffers	$V_{OL}$			0.1	$\text{V}$	$I_{OL} = 0 \text{ mA}$
High-level output voltage						
2.5V buffers	$V_{OH}$	$V_{DD} - 0.1$			$\text{V}$	$I_{OH} = 0 \text{ mA}$
3.3V buffers	$V_{OH}$	$V_{DD} - 0.1$			$\text{V}$	$I_{OH} = 0 \text{ mA}$

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