ASIC Technology

Product Letter

0.18 µm

CB-11 Cell-based CMOS ICs

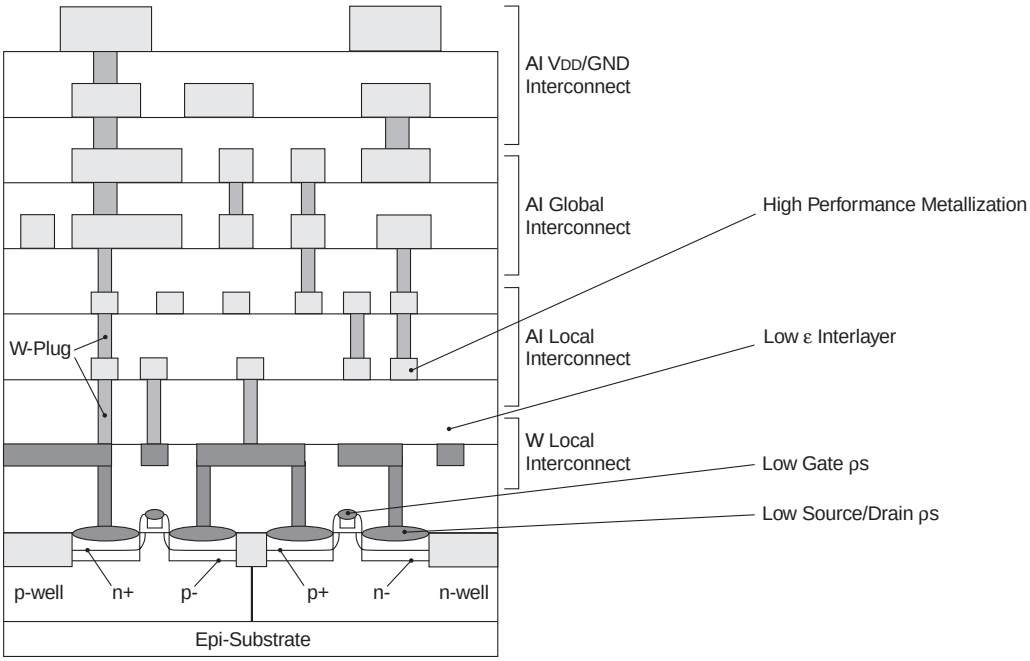
Description

NEC's 0.18 µm CB-11 family incorporates ultra-high performance, deep sub-micron cell-based ASIC's for high-end applications requiring high speeds, high integration density and low power dissipation.
The cell-based approach allows the most effective realization of true "system on a chip" applications. These may be composed of user-defined logic, high density memory, cores such as CPUs, DSPs or intelligent peripherals and analog-functions.

Features

- 0.18 µm (drawn, 0.15 µm effective) Cobalt-Silicide CMOS process
- Very large primitive libraries for excellent synthesis results
- Extensive support of state-of-the-art cores and interfaces
- Analog macro support such as DACs, ADCs, ...
- Available gate counts from 900 K to 45 million gates
- Extrememly low power dissipation of 0.015 µW/MHz/gate
- Optimized 1.8 V architecture
- Operation down to 1.5 V
- Special power rail structure
- Multi-oxide process enables full swing 3.3 V interfaces
- Ultra high pin count by using 30 µm pad pitch
- Flexible I/O structure supports LVDS, HSTL, GTL+, PCI, ...

Cross Section



System@IC
Solutions on a Chip

NEC

Product Outline

Master Name		µPD86xxx (30 die steps)
Available Gate Count (Raw)		900 K to 45100 K
Number of Pads (30µm Pitch)		396 to 2700
Toggle Frequency (Typ.)		2.6 GHz
Delay Time	Internal	27.3 ps (F/O = 2, l = 0 mm), 86.1 ps (F/O = 1, l = 0.25 mm)(F322)
	Input	58 ps (F/O = 2, l = 0 mm)(FI01)
	Output	1.320 ns (C_L = 50 pF)(FO02)
Consumed Power	Internal	0.015 µW/MHz/gate (1.8 V)
	Input	0.78 µW/MHz (F/O = 2, l = 0 mm)
	Output	61.04 µW/MHz (C_L = 15 pF)
Power Supply Voltage		1.8 V ± 0.15 V (operation down to 1.5 V possible)
Operating Temperature		-40 to +85° C
Interface Level		1.8V/3.3 V CMOS level, LVTTL level, GTL+,HSTL, PCI, pECL, AGP, SSTL
Technology		Standard cell 0.18 µm (0.15 µm effective) silicon gate CMOS; 7* Al-metal layers

*7th metal layer used for flip chip or power line.

Features

Architecture

The CB-11 ASICs are manufactured in NEC's advanced Cobalt-silicide (Co-Si) process. The chip layout is done using seven metal layers (Al). The use of area-pads for Flip-Chip BGA is enabled by the use of the topmost metal layer. As the CB-11 ASIC family follows a cell-based approach, it offers highest flexibility for power routing, split power supply lines and other customer specific requirements.

Memories

Nearly all advanced systems require memory support. Therefore, NEC has prepared a wide range of compiled memories. Single- and dual port synchronous memories in high-density, high-speed and super high-speed configurations are available. For largest on-chip memory, 4T-cell based SRAMs are supported.

Macros

In order to meet the demand for ever increased design efficiency, design-reuse is key. Therefore, NEC has prepared huge libraries of computing and communication cores. A broad selection of them will be supported as plug-and-play hard-macros for leading-edge CB-11 implementations.

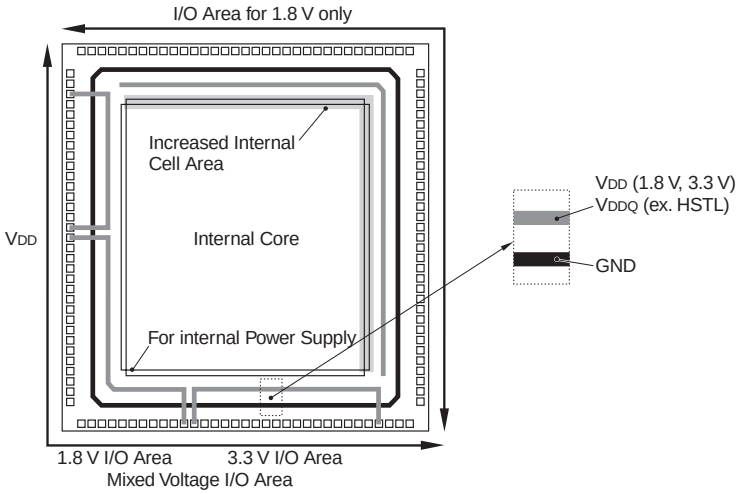
Interfacing

I/O Region

The CB-11 interface structure provides a variety of interface options. Although CB-11 is a 1.8 Volt optimized technology with thin gate oxide, NEC offers 3.3 Volt compatible I/O interfacing. The full swing 3.3 Volt interfacing can be achieved through a multi-oxide process in the I/O area. Using the power rail structure shown in the figure below, buffers for 1.8 Volt and 3.3 Volt interface levels can be mixed. The 1.8 Volt and 3.3 Volt buffers have different heights and therefore need different space in the I/O area. In case of pure 1.8 Volt I/O - as an example - the additional power rail for 3.3 Volt I/O can be omitted. In this case, the remaining area can also be used for internal cells. The result is an optimized and cost effective die size. The pure 1.8 Volt area is located here at the top and right side of the chip.

HSTL/PCI Interfacing

For designs using HSTL or PCI I/O blocks, the power rail structure described above supports the additional supply voltage of 1.4 Volt (VDDQ for HSTL) or 3.3 Volt (for PCI) in special power rails and pin assignment.



Further Publications

This product letter contains preliminary specifications and operational data for the CB-11 family. Additional information is available in NEC's CB-11 Design Manual, Block Library and other related documents.

Please contact your local NEC Design Center for further information; see the back of this product letter for locations and telephone numbers.

For further information on NEC's ASICs or other NEC products visit our European website at **www.nec.de**

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