

CB-C9VX/VM 0.35-Micron CMOS Cell-Based ASICs

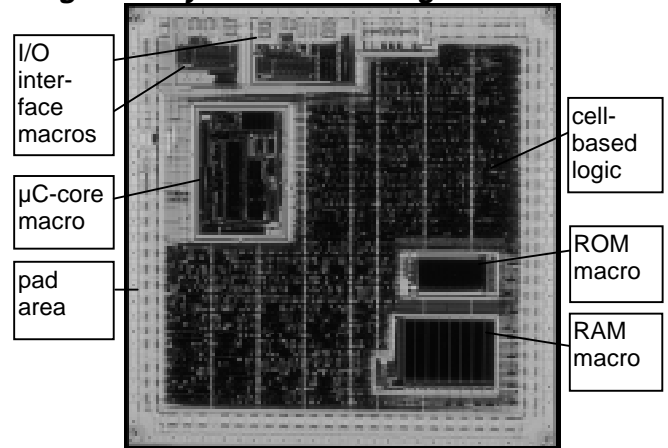
Description

The CB-C9VX/VM family offers ultra-high performance, deep submicron cell-based ASICs for high-end applications requiring high speeds, high integration density and low power dissipation. The CB-C9VX/VM family is the second generation of NEC's successful 0.35-micron (0.27-micron effective) silicon gate process.

The cell-based approach in conjunction with the superior electrical performance and the very high integration level allows the realisation of true "system-level-integration" applications (see Fig. 1). These may be composed of user-defined logic, complex predefined macro-functions such as microprocessors, digital signal-processors or intelligent peripherals and analog-functions. Of course the cell-based approach also allows the most effective integration of compiled memory macros.

Power sensitive applications make use of the low power dissipation of 0.37 $\mu\text{W}/\text{MHz}/\text{gate}$ at 3.3 V supply voltage and 100% switching rate. Very low power and hand-held applications are furthermore supported with a special 2 V library. The reduction of supply voltage leads to a power dissipation as low as 120 nW/MHz/gate.

Figure 1: System-Level-Integration



High speed applications also benefit from NEC's CB-C9VX/VM cell based ASIC family with an internal gate delay of 86 ps. This gate specification makes CB-C9VX/VM well suited for designs running up to 200 MHz.

Full 5V and 5V tolerant CMOS Interfaces

For those systems not yet ready to migrate completely to 3.3 V, CB-C9VM has full 5 V CMOS interfaces available. Applying two additional process steps, which realise a "multi-oxide" section in the I/O area, 5 V driving capabilities at full speed are available at the chip border with the help of a separate supply rail.

Table 1: CB-C9VX/VM Series Features and Benefits

CB-C9VX/VM Series Features	CB-C9VX/VM Series Benefits
• 0.35-micron (drawn) Ti-Silicide CMOS technology	⇒ Ultra high density cell structure
• Optimised 3.3 Volt transistor architecture	⇒ Highest speed at very low power consumption
• Very low power dissipation of 0.37 $\mu\text{W}/\text{MHz}/\text{gate}$	⇒ Fewer design limits, package constraints and supply current
• Multi- oxide section in I/O area with VM-option	⇒ Full-swing 5V I/Os with unchanged core performance
• Extensive logic-macro and memory-macro support	⇒ Cost effective system on silicon solutions
• Usable gate counts from 50k to 2736k gates	⇒ Support for a wide range of applications
• 26 base sizes, each with 2- and 3-ML options	⇒ Flexible base sizes to best fit design needs
• Three pad ring options for high pad-to-gate ratio	⇒ Minimum device cost for high I/O requirement
• Large I/O cell library including LVTTTL, HSTL, GTL, PCI...	⇒ Unrestricted, high performance system interfacing
• NEC's OpenCAD [®] design environment	⇒ Smooth and reliable design flow from customer design to silicon

In CB-C9VM the 5 V I/O buffers can be placed at any location of the I/O area and are freely mixable with 3.3 V buffers. The internal core is identical to CB-C9VX. However, in case the speed and drivability requirements of the 5 V I/O cells are moderate, CB-C9VX is flexible enough to offer as well 5 V tolerant I/Os, that safely interface to 5 V devices.

This unique feature is another step for highest design flexibility of system design.

Process

CB-C9VX/VM ASIC's are fabricated using NEC's 3.3 V 0.35 μm (drawn) titanium-silicide (Ti-Si) process. The Ti-Si option allows the use of a more compact cell layout, which results in a higher integration density compared to non-silicided CMOS processes. Signal wiring is done in two or three metal layers (Al). For this 2nd generation 0.35μm technology, the metal-2 routing within each cell is replaced with polysilicon, which significantly improves routability. The tightened metal pitch enables very low routing overhead. Thus, an excellent density of more than 17.5k available gates/mm² is achieved.

The CB-C9VX/VM ASIC family offers highest flexibility concerning power routing, split power supply lines and other customer specific requirements.

Integration Level

The CB-C9VX/VM family includes 26 different step sizes with die sizes from 4.5 x 4.5 mm² up to 19.54 x 19.54 mm². This results in a usable gate count from about 50k gates up to 2.7 mio gates.

To meet different design requirements, three different I/O pad geometries are defined. While pad structures with 60 μm pitch (C-Step type) offer highest I/O bandwidth for pad-limited designs, 120 μm pad structures (S-Step type) /- are well suited for core area limited designs. In between NEC's 80μm pad library (T-Step type) balances both requirements.

Table 2: CB-C9VX/VM line-up

Step Name	I/O Pads ¹ (C/T/S Step)	Usable Gates ²	
		2 layer	3 layer
B60	196/156/104	61 k	99 k
C02	236/180/124	71 k	137 k
C40	268/204/140	92 k	176 k
C78	300/228/156	131 k	219 k
D01	316/244/164	147 k	246 k
D26	340/260/176	162 k	274 k
D52	356/276/184	183 k	309 k
D90	388/300/200	211 k	361 k
E16	412/316/212	233 k	398 k
E54	444/340/228	263 k	460 k
E80	468/356/240	287 k	494 k
F18	500/380/256	317 k	562 k
F44	516/396/264	341 k	604 k
F70	540/412/276	366 k	638 k
G08	572/436/292	397 k	711 k
G34	596/452/304	422 k	755 k
G72	628/476/320	464 k	818 k
H10	660/500/336	493 k	893 k
H49	692/524/352	536 k	971 k
H87	726/548/368	579 k	1034 k
J26	758/572/384	607 k	1113 k
J51	772/588/392	629 k	1154 k
K15	828/628/420	714 k	1289 k
K92	892/676/452	802 k	1490 k
M97	1060/804/536	1141 k	2148 k
P63	1204/908/608	1433 k	2736 k

- 1 Depending on package and circuit specification, some pads are used for power only and are not available as signal pads
- 2 Actual gate count varies depending on circuit implementation, utilization and selection of C, T or S step

Block Library Support

NEC's CB-C9VX/VM ASIC family includes block library support which matches various different requirements. Huge libraries are available for both 3.3 V for highest performance and 2.0 V lowest power dissipation. For both voltages, libraries include cells for high drivability and for low power consumption, respectively, as shown in Tab.4. These cells can of course be mixed in one design. Design for Testability is supported by means of full-scan and LSSD library elements.

Table 3: Voltage Availability of CB-C9VX/VM

Library	CB-C9VX		CB-C9VM	
	I/O voltage	3.3 ±0.3V		5.0V ± 10%
core voltage	3.3 ± 0.3V	2.0 ± 0.2V	3.3 ± 0.3V	

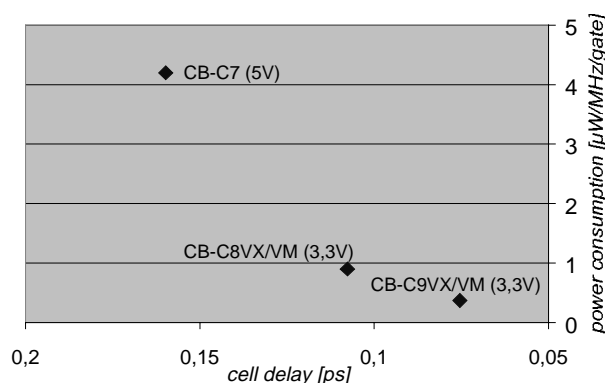
Each sub-library includes logic functions with several different drive strengths, allowing the synthesis tool to optimise the design according to the defined synthesis constraints.

Table 4: Block Libraries

Library	Combinational Logic Elements	Sequential Elements
High-speed	170	127
Low-power	161	86
Scan-Path	n/a	22

The CB-C9VX 3.3 V library features a typical gate delay of 75 ps for a 2-NAND gate with a fan-out of 1 and no wire load and a power dissipation of 0.37 $\mu\text{W}/\text{MHz}/\text{gate}$.

Figure 2: Performance Positioning of CB-C9VX/VM¹⁾



¹⁾ cell delay is the typical delay time of F322 NAND2 with a F/O of 1 and no wire load; power consumption is a typical value

For very low power applications, the CB-C9VX family also supports 2 V core supply voltage. The trade-off is a decreased timing performance with a 151 ps gate delay for 2-NAND with fanout of 1 and no wire load. The big advantage of this 2 V library is a reduced power consumption of 120 $\mu\text{W}/\text{MHz}/\text{gate}$.

Macro Library Support

The high integration density in conjunction with the large silicon die size and the ultimate design flexibility offered by NEC's CB-C9VX/VM technology builds the foundation for complete system level integration. This trend is driven by NEC with a strong support for large predefined macro blocks which in many cases represent the functionality of well known standard devices.

A subset of the available macros is shown in Table 5. The macro library is under steady growth and NEC also offers a macro on demand service based on customer requests.

The macros are completely supported by NEC's OpenCAD[®] environment, which includes high quality simulation and test pattern generation support.

Of course various kinds of memory macros are also available for CB-C9VX/VM. Memory blocks are generated based on advanced memory-compiler tools and thus ensure highest flexibility according to customer requirements. Available memory types include single and dual port RAM macros optimised either for speed or density and asynchronous ROM.

Technical data from compiled RAM blocks are summarised in Table 6 on the next page for 3.3 V supply voltage.

Content addressable memories (CAM) can be a very efficient way of implementing algorithms as comparisons for data filtering and translations, as often used for applications in data management, networking or compression. NEC offers a high performance CAM macro allowing highest flexibility for optimum system design.

As process technology of CB-C9VX/VM is compatible to 1st generation technology, all macros and library elements of this family are available, as well.

Table 5: CB-C9VX/VM Mega Macro Library (subset listing)

Type	Description	Type	Description
analog	A/D Converter: 10 bit, 100 KHz	I/F Periph.	NA71037L: DMA Controller
analog	A/D Converter: 8 bit, 100 KHz	I/F Periph.	NA71051L: USART, 300kBit/s, full duplex
analog	A/D Converter: 8 bit, 500 KHz	I/F Periph.	NA71054L: progr. timer/counter
analog	A/D Converter: 8 bit, 220 MHz	I/F Periph.	NA71055L: progr. parallel interface (3x 8bit)
analog	Triple D/A Converter: 8 bit, 220 MHz	Datapath	High-Speed Multiplier/Accumulator
analog	D/A Converter: 8 bit, 220 MHz	CPU	V30MX: 16 bit/33 MHz microprocessor
analog	D/A Converter: 9 bit, 5 MHz	CPU	NZ70008H: 8 bit/16 MHz Z80 microprocessor
analog	D/A Converter: 10 bit, 30 MHz	CPU	V850E: 32 bit RISC microcontroller
PLL	Analog PLL	DSP	OAK: Digital Signal Processor
I/F Periph.	USB: Universal Serial Bus Interface	DSP	PINE: Digital Signal Processor
I/F Periph.	RAC: RAMBUS ASIC Cell	DSP	SPX
I/F Periph.	NA71059L: progr. interrupt controller	CPU	ARM7TDMI
I/F Periph.	IEEE 1284: Bidirectional Centronics	CPU	V30MT: microprocessor
I/F Periph.	NA16550: UART with FIFO	CPU	V810: RISC microcontroller
I/F Periph.	NA4993: 8 bit parallel I/O real-time clock	CPU	V851: RISC microcontroller

Table 6: Compiled RAM Specification

RAM Type	3.3 Volt supply voltage		min. size [bits x words]	max. size ²⁾ [bits x words]
	T _{ac} ¹⁾ [ns]	P _{dyn} [mW/MHz]		
1-port High-Speed	3.61	0.50	1 x 32	32 x 2048
1-port High-Density	6.50	0.36	1 x 16	32 x 2048
1-port Super High-Speed	2.89	0.34	1 x 64	16 x 1024
2-port High-Speed	3.73	0.97	1 x 32	32 x 2048
2-port High-Density	7.41	0.50	1 x 32	32 x 1024

¹⁾ max. access time at 8bits x 512 words from clock to valid data with unloaded outputs

²⁾ larger block sizes are available by connecting basic hard macros

Interface Macro Support

The CB-C9VX/VM standard interface library includes complete LVTTTL input, output and bidirectional buffer support with optional schmitt-trigger, pull-up and pull-down support.

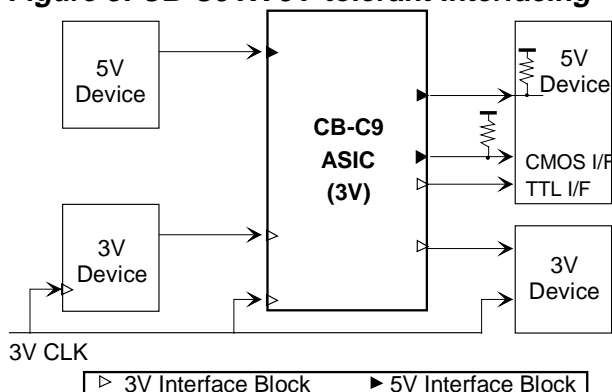
For very low power applications additional level shifter cells are available which allow the usage of 3.3 V I/O interfaces for system compatibility in conjunction with 2 V core supply voltage.

For special applications a set of high-speed I/O buffer types is available. This includes 3.3 V PCI Cells for 66 MHz applications, GTL (Gunning Transceiver Logic) I/O cells, HSTL (class 1, 2, 3, 4) interface cells and pseudo-ECL (pECL) input cells.

5V tolerant I/Os with CB-C9VX

Although CB-C9VX is a 3.3 V optimised technology with thin gate oxide, NEC offers 5 V compatible I/O interfacing. As Figure 3 shows, NEC's interface library allows direct interfacing to 5 V devices on input and output side. Output levels are compatible to 5 V TTL specification, input levels are compatible to 5 V CMOS and TTL specification and both are internally protected against damaging. For such applications no additional 5 V supply voltage is necessary.

Figure 3: CB-C9VX 5V-tolerant Interfacing



CB-C9VX/VM Applications

Major advantages of NEC's CB-C9VX/VM ASIC family are high integration density, high speed, very low power consumption and cost effective memory and megamacro integration.

Following these main advantages results in a wide range of applications. High performance transmission and switching systems for example based on ATM technique may take advantage from high speed, high integration density and high performance memory integration. High end hand-held applications as PDA's or mobile communication equipment make use of low power and the capability of global system integration including powerful microprocessor cores, which results in small system cases. Future high end consumer products such as digital TV set-top boxes need system on silicon integration to allow cost effective mass production. High end chipsets for engineering work stations (EWS) or graphic PC-subsystems need very high performance combined with cost effective packaging solutions. So the very low power consumption offered by NEC's CB-C9VX/VM family has impact on system pricing, as in many cases the usage of more cost effective packaging solutions becomes possible.

CAD Support

The CB-C9VX/VM family ASIC's are completely supported by NEC's OpenCAD™ design environment, a unified front-to-back-end design package that allows designers to mix and match tools from the industry's most popular third-party vendors and from NEC's

offering of powerful proprietary software tools. These tools perform schematic capture, logic synthesis, floor-planning, logic and timing simulation, static timing analysis, layout, design and circuit rule check, and memory compilation. The company's proprietary clock tree synthesis tool can be used to automatically buffer the clock lines as needed to minimise clock skew, essential for high speed designs.

The library elements of NEC's CB-C9VX/VM family are modelled in a non-linear way using table look up methods. This allows the most accurate timing verification throughout synthesis, estimated timing simulation and sign-off timing simulation as it includes not only the influence of actual load conditions but also of the logic-cells input slopes. NEC spends most efforts to guarantee a converging design flow and to avoid design iterations.

Placement and routing is performed in NEC's European headquarter in Düsseldorf (Germany), which allows quick and flexible handling of specific design demands. In most cases no floorplanning is necessary, to meet the required timings. This leads to a significant reduction of design efforts on the customer's side. For complex hierarchical designs, NEC's floorplanner may be used to speed design time and ensure critical paths.

Test Support

The CB-C9VX/VM family supports automatic test generation through a scan-test methodology, which allows high fault coverage, easy testing and short development time. This includes internal scan as well as boundary scan. NEC also offers optional build-in self test (BIST) architecture for RAM testing. Test of embedded megamacros is supported from NEC's testbus concept, which allows the use of predefined test pattern sets for integrated core macros.

Packaging

NEC offers a wide variety of over 60 package types. The CB-C9VX/VM family can be packaged in NEC's most popular packages. These include plastic quad-flat packs (PQFPs)

with optional head spreader and pin counts in the range from 100 to 304 pins. Plastic Ball Grid Arrays (BGA) and Tape BGAs 256 to 696 ball contacts and Fine Pitch BGAs with 0.8 μm ball pitch are also supported.

Clear Roadmap

NEC's technology portfolio offers a clear roadmap of advanced process technologies and its library support. For long-running products, NEC guarantees to produce the ASIC devices as long as the customer requires them. For leading-edge devices, NEC always offers industry-leading technologies to get highest output.

Publications

This data sheet contains specifications, package information, and operational data for the CB-C9VX/VM cell based ASIC family. Additional design information is available in NEC's ASIC selection guide, CB-C9VX/VM block library and design manual. Please contact your local NEC Design Center for further information.

CB-C9VX Performance

Overview Absolute Maximum Ratings

Power supply voltage, V_{DD}	-0.5 to 4.6 V
Input voltage, V_I	
3V input buffer (at $V_I < V_{DD} + 0.5$ V)	-0.5 to 4.6 V
3V fail-safe input buffer (at $V_I < V_{DD} + 0.5$ V)	-0.5 to 4.6 V
5V-tolerant buffer (at $V_I < V_{DD} + 3.0$ V)	-0.5 to 6.6 V
Output voltage, V_O	
3V buffer (at $V_O < V_{DD} + 0.5$ V)	-0.5 to 4.6 V
5V-tolerant buffer (at $V_O < V_{DD} + 3.0$ V)	-0.5 to 6.6 V
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Input/Output Capacitance $V_{DD}=V_I=0$ V; $f=1$ MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Note: Values do not include package pin capacitance.

Power Consumption

Description	Limits	Unit
2-input NAND (F302, F/O=0, I=0)	0.37	μ W/MHz
2-input NAND (F302, F/O=2, I=typ)	0.63	μ W/MHz

Recommended Operating Conditions

Parameter	Symbol	3V Buffer		5V-Tolerant		3.3V PCI		Unit
		Min	Max	Min	Max	Min	Max	
Power supply voltage	V_{DD}	3.0	3.6	3.0	3.6	3.0	3.6	V
Junction temperature	T_J	-0	+125	-0	+125	-0	+125	°C
Low-level input voltage	V_{IL}	0	0.8	0	0.8	-0.5	0.3 V_{DD}	V
High-level input voltage	V_{IH}	2.0	V_{DD}	2.0	V_{DD}	0.5 V_{DD}	$V_{DD}+0.5$	V
Input rise or fall time	t_R, t_F	0	200	0	200	0	200	ns
Input rise or fall time, Schmitt	t_R, t_F	0	10	0	10	0	200	ms

AC Characteristics $V_{DD} = 3.3$ V \pm 0.3 V; $T_J = 0$ to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	880			MHz	D-F/F; F/O=2, L=0
Delay time						
2-input NAND (F322)	t_{PD}	49.8	76.1	113.2	ps	F/O=1; L=0
	t_{PD}	76.6	113.8	169.9	ps	F/O=2; L=typ
Flip-flop (F611NQ)	t_{PD}	321.4	497.4	776.1	ps	F/O=1; L=0
	t_{PD}	354.2	549.6	860.0	ps	F/O=2; L=typ
	t_{SETUP}	490			ps	—
	t_{HOLD}	390			ps	—
Input buffer (FI01)	t_{PD}	107.4	155.6	221.9	ps	F/O=1; L=0
	t_{PD}	126.7	175.5	252.0	ps	F/O=2; L=typ
Output buffer (12 mA) 3.3V	t_{PD}	454.5	675.5	1021	ps	$C_L = 0$ pF
Output buffer (12 mA) 3.3V	t_{PD}	1624	2375	3525	ps	$C_L = 50$ pF
Output buffer (6 mA) 5V-tolerant	t_{PD}	957	1393	2078	ps	$C_L = 0$ pF
Output buffer (6 mA) 5V-tolerant	t_{PD}	2508	3650	5408	ps	$C_L = 50$ pF
Output rise time (9 mA)	t_R	1708	2165	2994	ps	$C_L = 15$ pF; 10-90%
Output fall time (9 mA)	t_F	1082	1522	2381	ps	$C_L = 15$ pF; 10-90%

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